AMENDMENTS TO THE CLAIMS

Claims 1-23 are pending. Please amend claims 4, 9 and 14 as set forth below, without acquiescence in the Office Action's reasons for rejection or prejudice to pursue in a related application. Claims 16-23 are new. No new matter has been added.

1. (Previously Presented) A method for determining a worst-case transition comprising:

determining at least a plurality of slews of output timing events for a plurality of input timing events based on a timing model of a gate; and

selecting a worst-case input timing event from the plurality of input timing events based on at least the slews of the output timing events.

2. (Original) The method of claim 1, further comprising:

determining a plurality of gate delays for a plurality of input signals based on the timing model of the gate.

3. (Previously Presented) The method of claim 2, wherein selecting a worst-case input timing event further comprises:

selecting a worst delay based on the gate delays.

4. (Currently Amended) The method of claim 1, wherein the timing model comprises:

$T_o = T_i + D_g$,

$D_g = F(S_i, C)$,

$S_o = Q(S_i, C)$;

~~$T_o = Q(T_i, D_g)$;~~

where T_o is an output time, T_i is an input time, D_g is a gate delay, S_i ~~T_i~~ is an input slew, C ~~L~~ is a capacitive load of the gate, and S_o ~~T_o~~ is an output slew, wherein the delay D_g of the gate depends, at least in part, on the slew of the input transition and the capacitive load at the output of the gate.

5. (Original) The method of claim 1, wherein the timing model is a timing library format (TLF) model.

6. (Previously Presented) An apparatus for determining a worst case transition comprising:

means for determining at least a plurality of output slews for a plurality of input signals based on a timing model of a gate; and

means for selecting a worst delay input signal from the plurality of input signals based on at least the output slews.

7. (Original) The apparatus of claim 6, further comprising:

means for determining a plurality of gate delays for a plurality of input signals based on the timing model of the gate.

8. (Previously Presented) The apparatus of claim 7, wherein said means for selecting a worst-case input timing event further comprises:

means for selecting a worst delay based on the gate delays.

9. (Currently Amended) The apparatus of claim 6, wherein the timing model comprises:

$T_o = T_i + D_g$,

$D_g = F(S_i, C)$,

$S_o = Q(S_i, C)$;

~~$T_o = Q(T_i, D_g)$;~~

where T_o is an output time, T_i is an input time, D_g is a gate delay, S_i ~~T_i~~ is an input slew, C ~~L~~ is a capacitive load of the gate, and S_o ~~T_o~~ is an output slew, wherein the delay D_g of the gate depends, at least in part, on the slew of the input transition and the capacitive load at the output of the gate.

10. (Original) The apparatus of claim 6, wherein the timing model is a timing library format (TLF) model.

11. (Previously Presented) A computer readable medium storing a computer program comprising instructions which, when executed by a processing system, cause the system to perform a method for determining a worst case transition, the method comprising:

determining at least a plurality of output slews for a plurality of input signals based on a timing model of a gate; and

selecting a worst delay input signal from the plurality of input signals based on at least the output slews.

12. (Original) The medium of claim 11, further comprising instructions, which, when executed by the processing system, cause the system to perform the method for determining a worst case transition, the method further comprising:

determining a plurality of gate delays for a plurality of input signals based on the timing model of the gate.

13. (Previously Presented) The medium of claim 12, further comprising instructions, which, when executed by the processing system, cause the system to perform the method for determining a worst case transition, wherein selecting a worst-case input timing event further comprises:

selecting a worst delay based on the gate delays.

14. (Currently Amended) The medium of claim 11, wherein the timing model comprises:

$T_o = T_i + D_g$,

$D_g = F(S_i, C)$,

$S_o = Q(S_i, C)$;

~~$T_e = Q(T_i, D_g)$;~~

where T_o is an output time, T_i is an input time, D_g is a gate delay, S_i ~~T_i~~ is an input slew, C ~~L~~ is a capacitive load of the gate, and S_o ~~T_e~~ is an output slew, wherein the delay D_g of the gate depends, at least in part, on the slew of the input transition and the capacitive load at the output of the gate.

15. (Original) The medium of claim 11, wherein the timing model is a timing library format (TLF) model.

16. (New) The method of claim 1, wherein the slews of the output timing events include slew rates of the output timing events, which is determined by an amount of time for a waveform to transition from a first voltage level to a second voltage level.

17. (New) The apparatus of claim 6, wherein the output slews of the output timing events include output slew rates of the output timing events, which is determined by an amount of time for a waveform to transition from a first voltage level to a second voltage level.

18. (New) The medium of claim 11, wherein the output slews of the output timing events include slew rates of the output timing events, which is determined by an amount of time for a waveform to transition from a first voltage level to a second voltage level.

19. (New) A method for determining a worst-case timing event comprising:

determining a plurality of output arrival times and slew rates for a plurality of input timing events based on a timing model and a capacitive load of a gate; and

selecting a worst-case input timing event from the plurality of input timing events based on the output arrival times and slew rates determined on the output of the gate.

20. (New) The method of claim 19, further comprising:

determining a plurality of gate delays for a plurality of input signals based on the timing model of the gate.

21. (New) The method of claim 20, wherein selecting a worst-case input timing event further comprises:

selecting a worst delay based on the gate delays.

22. (New) The method of claim 19, wherein the timing model comprises:

$$T_o = T_i + D_g,$$

$$D_g = F(S_i, C),$$

$$S_o = Q(S_i, C);$$

where T_o is an output time, T_i is an input time, D_g is a gate delay, S_i is an input slew, C is a capacitive load of the gate, and S_o is an output slew, wherein the delay D_g of the gate depends, at least in part, on the slew of the input transition and the capacitive load at the output of the gate.

23. (New) The method of claim 19, wherein the timing model is a timing library format (TLF) model.